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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/789,033	02/27/2004	Michael Bauer	1431.103.101/FIN 423 US	8344

7590 11/01/2007
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EXAMINER

SEFER, AHMED N

ART UNIT	PAPER NUMBER
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2826

MAIL DATE	DELIVERY MODE
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11/01/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/789,033

Applicant(s)

BAUER ET AL.

Examiner

A. Sefer

Art Unit

2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 September 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 6-14 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 6-14 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9/20/2007 has been entered.

Specification

2. Claim 14 is objected to because of the following informalities: The recitation calling for, "the semiconductor chip" should read "the semiconductor chips". Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 13 and 14 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claim 14 recites the limitation "the contact pads." There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 6-12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakajima JP 2002-299372 (of record) in view of Malhi et al. ("Malhi") USPN 5,031,072.

Nakajima discloses figs. 1-6 a semiconductor chip 20 with a top side, a rear side opposite to the top side, and edge sides (fig. 4), the semiconductor chip comprising an integrated circuit 1 on the top side; at least one edge side having edge contacts 6 wherein the edge contacts extend from the top side in the direction of the rear side of the semiconductor chip; wherein the edge contacts are connected to electrodes 3 of the integrated circuit via conductor tracks (the narrow wiring portion on the top edge of element 6 connecting elements 6 and 3 shown in figs. 2 and 4) located on the top surface of the semiconductor chip, but does not disclose a circuit substrate having a top side with external contacts.

Malhi discloses 1-17 a plurality of semiconductor chips 12 with a top side, a rear side opposite to the top side; and a circuit substrate having a top side with external contacts 22, wherein the semiconductor chips are electrically connected via the edge contacts 18/20/28 among one another and also with respect to the external contacts on the circuit substrate such that the top and rear sides of the semiconductor chips are oriented perpendicular to the top side of the circuit substrate.

Therefore, in view of Malhi's teachings, one having an ordinary skill in the art at the time the invention was made would be motivated to modify Nakajima by incorporating a circuit substrate having a top side with external contacts. The motivation would be to allow multiple integrated circuit chips to be packaged in a space much smaller than packaging schemes heretofore known as taught by Malhi (col. 10, lines 10, lines 60-667).

Re claims 7 and 8, Nakajima discloses edge sides having a perforation-like structure, semicylinder-like cutouts extending as edge contacts from the top side in the direction of the rear side (figs. 2 and 4), and having a metal layer 6 (fig. 3) or an insulating layer 5 (as in claim 8).

Re claim 9, Nakajima discloses cutouts having a soldering material 31 (e.g. nickel/gold, see page 4, par. 2.1 of machine translated document).

Re claim 10, Nakajima discloses edge contacts being extended on the top side to form a contact area 3 and merge with a conductor track (fig. 2) on the top side.

Re claim 11, Malhi discloses (col. 10, lines 46-59) semiconductor chips arranged on the circuit substrate within an electronic component.

Re claim 12, Malhi discloses external contacts on the top side of the circuit substrate being a conductor track structure having line running in parallel.

Re claim 14, Malhi discloses the semiconductor chip 12 being arranged with an edge side on the circuit substrate, the top side of the chip being arranged in angular fashion wrt the top side of the substrate and the edge contacts being electrically connected to the conductor structure via contact pads 22 on the top side of the circuit substrate.

Claim Rejections - 35 USC § 103

8. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakajima in view of Malhi as applied to claim 6 and 12 and in further in view of Koike et al. ("Koike") WO 03/012868.

The combined references disclose the device structure as recited in the claim but does not disclose a plastic composition.

Koike discloses the employment of an insulating plastics 5 arranged on a circuit substrate in a manner embedding edge sides of the chip and contact pads 4.

It would have been obvious to employ a plastic composition so as to provide a better protection of the device from moisture and dust.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (571) 272-1921.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272-1236.

Application/Control Number:
10/789,033
Art Unit: 2826

Page 6

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ANS
October 29, 2007



A. Sefer
Patent Examiner
Art Unit 2826